ABSTRACT OF THE DISCLOSURE

In an SRAM, memory cells are each constructed of four NMOS transistors and two PMOS transistors 25 and 26. The four NMOS transistors are each constructed of DTMOS in which the channel region is electrically connected to the gate. In each NMOS transistor, a threshold voltage Vth is lower in an ON stage than in an OFF stage. The threshold voltage Vth in the OFF stage is equivalent to that of an ordinary NMOS transistor in which the channel region is not electrically connected to the gate. Read and write circuits of the SRAM also include MOS transistors formed of DTMOS in which the channel region is electrically connected to the gate.